AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 9, 16, 19 and 20 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit configured to calculate and present an output signal having a first resolution and a plurality of output pixels in response to (i) an input signal having a second resolution and a plurality of input pixels and (ii) one or more control signals, wherein said input signal is ~~received~~ stored in a register file a scan line at a time in response to a data request signal; and

a second circuit configured to generate said control signals in response to (i) a previous calculation by said first circuit and (ii) one or more input parameters, wherein said first circuit is configured to scale and filter said input signal to allow one or more of said input pixels to contribute to the creation of one or more of said output pixels, wherein said apparatus comprises a portion of a block move engine (BME).

2. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said ~~input signal comprises a 3-component video signal~~ first circuit further comprises a multiplexer configured to generate said output signal by selecting said plurality of input pixels from said register file in response to said one or more control signals.

3. (CURRENTLY AMENDED) The apparatus according to claim ~~1~~ 2, wherein said ~~input signal comprises a 3-component video signal with a separate alpha component~~ register file comprises a plurality of register sets configured to provide said plurality of input pixels to said multiplexer.

4. (ORIGINAL) The apparatus according to claim 1, wherein said first circuit independently calculates a horizontal component and a vertical component of said output signal.

5. (CANCELED)

6. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to operate on one or more blocks of data.

7. (CURRENTLY AMENDED) The apparatus according to claim ~~6~~ 1, wherein said ~~apparatus is configured to read a block of data a scan line at a time~~ second circuit comprises a filter control circuit configured to generate said one or more control signals and said data request signal in response to one or more filter control signals, wherein said filter control signals provide (i) the size of a filter aperture, (ii) a linear scaling ratio, and (iii) a first output pixel position relative to input data.

8. (CURRENTLY AMENDED) The apparatus according to claim ~~7~~1, wherein said apparatus is configured to (i) process said scan line, (ii) write said scan line back to ~~said~~ a memory and (iii) process a next scan line.

9. (CANCELED)

10. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said apparatus is configured to allow two or more of said input pixels to contribute to the creation of one or more of said output pixels.

11. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to scale alpha data associated with an image.

12. (CURRENTLY AMENDED) An apparatus comprising:

means for calculating an output signal having a first resolution and a plurality of output pixels in response to (i) an input signal having a second resolution and a plurality of input pixels and (ii) one or more control signals, wherein said input signal is ~~received~~ stored in a register file a scan line at a time;

means for generating said control signals in response to (i) a previous calculation by said means for calculating and (ii) one or more input parameters; and

means for scaling and filtering said input signal to allow one or more of said input pixels to contribute to the creation of one or more of said output pixels, wherein said apparatus comprises a portion of a block move engine (BME).

13. (CURRENTLY AMENDED) A method for scaling and filtering of video, comprising the steps of:

(A) calculating an output signal having a first resolution and a plurality of output pixels in response to (i) an input signal having a second resolution and a plurality of input pixels and (ii) one or more control signals, wherein said input signal is ~~received~~ stored in a register file a scan line at a time in response to a data request signal;

(B) generating said control signals in response to (i) a previous calculation by step (A) and (ii) one or more input parameters; and

(C) scaling and filtering said input signal to allow one or more of said input pixels to contribute to the creation of one or more of said output pixels, wherein the method is implemented in a block move engine (BME).

14. (CURRENTLY AMENDED) The method according to claim 13, wherein ~~said input signal comprises a 3-component video signal~~ step (A) further comprises the step of:

selecting said plurality of input pixels from said register file in response to one or more control signals.

15. (CURRENTLY AMENDED) The method according to claim 13, wherein ~~said input signal comprises a 3-component video signal with a separate alpha component~~ step (B) further comprises:

generating said control signals and said data request signal in response to one or more filter control signals wherein said filter control signals provides (i) the size of a filter aperture, (ii) a linear scaling ratio and (iii) a first output pixel position relative to input data.

16. (CANCELED)

17. (PREVIOUSLY PRESENTED) The method according to claim 13, further comprising the step of:

operating on one or more blocks of data.

18. (CURRENTLY AMENDED) The method according to claim ~~17~~13, further comprising the step of:

reading a block of data a scan line at a time.

19. (CANCELED)

20. (CANCELED)

21. (PREVIOUSLY PRESENTED) The method according to claim 13, further comprising the step of:

allowing one or more input pixels to contribute to the creation of two or more output pixels.

22. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, further comprising:

a microprocessor coupled to said second circuit through a bus.

23. (NEW) The apparatus according to claim 1, wherein said second circuit comprises a coefficient RAM circuit configured to provide (i) a color coefficient for an input color pixel and (ii) an alpha coefficient for an input alpha pixel.

24. (NEW) The apparatus according to claim 23, wherein said second circuit comprises a color multiplier and accumulator (MAC) configured to (i) multiply said color coefficient to said input color pixel and (ii) produce a first result.

25. (NEW) The apparatus according to claim 24, wherein said second circuit comprises an alpha MAC configured to (i) multiply said alpha coefficient to said input alpha pixel and (ii) produce a second result.

26. (NEW) The apparatus according to claim 1, wherein said second circuit comprises an output register configured to (i) store a final output between the summation of a first result and

value and (ii) store a final output between the summation of a second result and value.